EE356A-Lab 3

Class E RF PA

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Due date

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Objective

This lab aims to analyze the operating behavior of a Class E switched-mode power amplifier operating at high frequencies. You will use simulations in LTSPICE and experiments to obtain the power transfer characteristics and efficiency at different frequencies and input voltages.

The lab consist of three parts:

1. **Converter Design and simulation** (Chapter 1)
2. **Inductor fabrication and PCB assambly** (Chapter 2):
3. **Experimental Characterization of the power amplifier** (Chapter 3):

Problem 1

Converter Design and simulation

A simplified schematic of the Class-E RF power amplifier (N. O. Sokal and Sokal 1975) you will implement in the laboratory is shown in Figure 1.1.

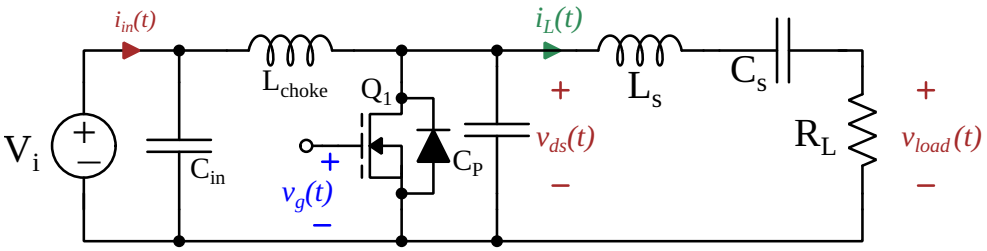


Figure 1.1: Class-E switched mode power amplifier

1.1 Class-E amplifier design and initial simulation

Following the design guidelines discussed in the lecture, determine the component values required to design a Class-E inverter that meets the specifications listed in Table 1.1.

Table 1.1: Class-E specifications

Parameter	Value	Units
f_s	6.78	MHz
V_i	12	V
R_{load}	5	Ω

In the idealized Class-E inverter shown in Figure 1.1, the choke inductor L_{choke} is assumed to be very large, allowing the input current $i_{in}(t)$ to be considered constant. In practice, however, a finite and realizable inductance must be used. For the Class-E inverter constructed in this laboratory, you may assume a choke inductance satisfying

$$L_{choke} \geq 5 \times L_s$$

For your design, assume that the gate drive signal $v_g(t)$ is square-wave with sufficient amplitude to fully enhance the switch and a fixed duty cycle of 50%.

Complete the following tasks:

- ☐ Simulate your design using LTSPICE with an ideal switch.
- ☐ Provide a list of all component values used in your design.
- ☐ Plot three full cycles of the following steay-state waveforms: $v_g(t), v_{ds}(t)$ and $v_{load}(t)$.
- ☐ Report the simulated output power and the ratio $\frac{\max(v_{ds}(t))}{V_i}$.

1.2 Matching network design and updated simulation

Although the class-E in Chapter 1 is designed for a $5\ \Omega$ load, a $50\ \Omega$ RF attenuator will be used in the laboratory to enable more accurate performance measurements. Consequently, you must design a 6.78 MHz, matching network that transforms a $50\ \Omega$ load to an effective $5\ \Omega$ load, as shown in Figure 1.2.

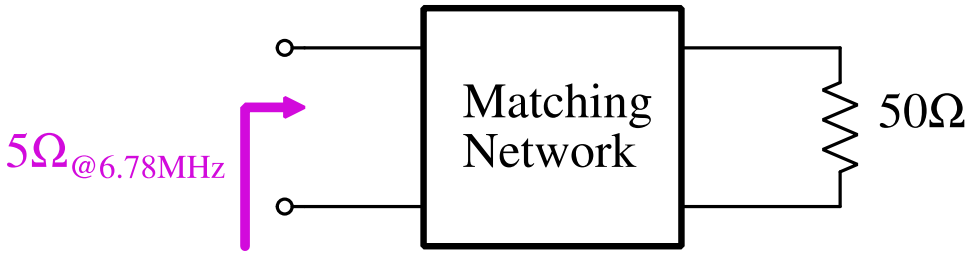


Figure 1.2: Matching network

Update your LTSPICE simulation to include the matching network. Note that some elements of the matching network may be combined with the resonant components of the Class-E amplifier, thereby reducing the total number of components required.

Complete the following tasks:

- ☐ Provide the component values of your 6.78 MHz, $50\ \Omega$–to–$5\ \Omega$ matching network.
- ☐ List the component values of the updated design, clearly indicating any combined elements.
- ☐ Plot three full cycles of the steady-state waveforms $v_g(t)$, $v_{ds}(t)$, and $v_{load}(t)$. In this simulation, the load resistance should be $50\ \Omega$.
- ☐ Report the simulated output power and the ratio $\frac{\max!(v_{ds}(t))}{V_i}$.
- ☐ Briefly discuss the differences between the simulation results with and without the matching network.

Problem 2

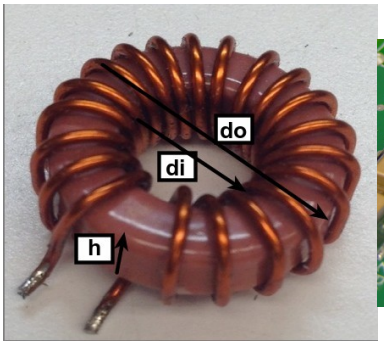
Inductor fabrication and PCB assambly

2.1 Inductor Design and Characterization

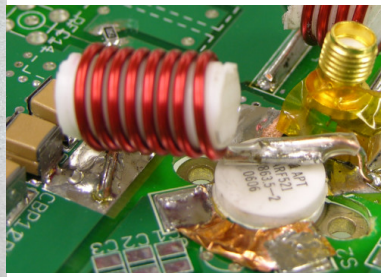
In this lab, you will fabricate your own air-core inductors. You will use magnet wire to manually wind either toroidal air-core inductors (Figure 2.1a) and/or solenoidal inductors (Figure 2.1b).

After fabrication, you will measure their impedance over frequency and extract the parasitic component values of the equivalent circuit model shown in Figure 2.1c. Incorporating these parasitics into your simulation will improve agreement between simulated and experimental results.

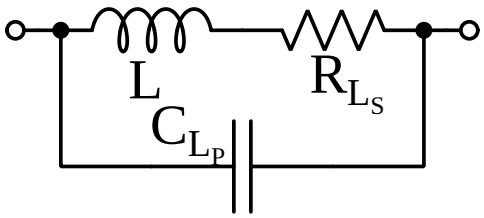
Therefore, aim to fabricate inductors whose nominal inductance values closely match those used in your simulation.



(a) Wire wound air core toroid.



(b) Wire wound air core toroid.



(c) Equivalent inductor model

Figure 2.1: Aircore torodial Inductor and equivalent circuit model

2.1.1 Toroidal inductor design

The inductance of a toroidal air-core inductor such as the one shown in Figure 2.1a is given by

$$L = \underbrace{\frac{N^2 h \mu_0}{2\pi} \ln\left(\frac{d_o}{d_i}\right)}_{\text{toroidal component}} + \underbrace{\frac{d_i + d_o}{4} \mu_0 \left[\ln\left(8\frac{d_o + d_i}{d_o - d_i}\right) - 2\right]}_{\text{single-turn loop component}} \tag{2.1}$$

where:

- $N =$ number of turns

- d_o = outer diameter
- d_i = inner diameter
- h = height
- μ_0 = permeability of free space

2.1.2 Solenoidal inductor design

For solenoidal air core inductor (see Figure 2.2), you may use the equation attributed to Harold A. Wheeler:

$$L = \frac{a^2 N^2}{9a + 10b} \tag{2.2}$$

where:

- L = inductance in μH
- a = coil radius (inches)
- b = coil length (inches)
- N = number of turns

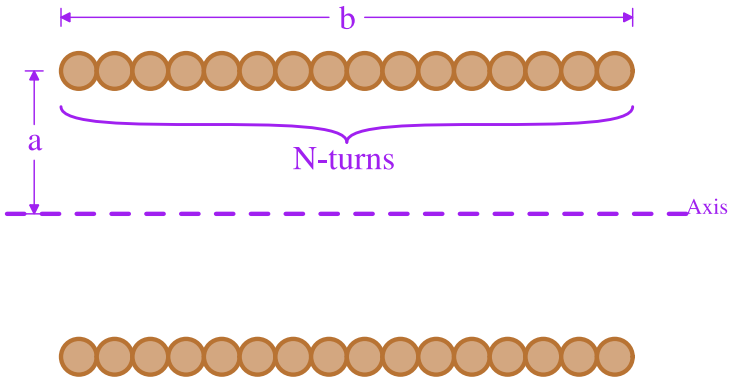


Figure 2.2: Wire wound air-core solenoid.

Equation 2.1 and Equation 2.2 assume ideal winding geometry and are more accurate when the number of turns is large. For this lab, treat these equations as *approximate design tools* to determine initial coil dimensions.

You may use a plastic form, rod, or a 3D-printed former for winding your inductors. Achieving the exact target inductance will likely require iterative measurement and adjustment of the winding count and geometry.

2.1.3 Inductor Measurement

Measure the impedance of your inductors over a frequency range spanning one decade below and one decade above the switching frequency. Since $f_s = 6.78$ MHz, an appropiate measurement range is

$$1\ \text{kHz} \leq f \leq 100\ \text{MHz}$$

The impedance Bode plot should resemble the response of the equivalent model in Figure 2.1c. Use your measured magnitude and phase data to extract the parameters of the equivalent circuit model that best fit the experimental impedance.

You will use the NanoVNA to perform these measurements. **Be sure to calibrate the NanoVNA before taking measurements.**

Complete the following tasks:

- ☐ Using the NanoVNA, measure and plot the impedance magnitude (in dB) and phase over 1 kHz $\leq f \leq$ 100 MHz.
- ☐ Extract and report the parameters of the equivalent circuit model shown in Figure 2.1c.

2.2 Nonlinear C_{oss} of Si MOSFET

In this lab, you will use the BSC065N06LS5 Si MOFSET from Infineon Technologies. The datasheet and links to the BSC065N06LS5 Si device, as well as links to the device spice models can be found here.

The MOSFET exhibits a nonlinear drain–source capacitance (C_{oss}) that varies with the applied drain–source voltage v_{ds}. The capacitance variation is shown in Figure 2.3 (Plot #11 in the datasheet).

A common approach to account for this nonlinearity in hand design is to approximate the device with a constant capacitance equal to the nonlinear capacitance evaluated at the average drain voltage: %$C_{oss}(v_{ds})|_{\langle V_{DS} \rangle}$$

> **Note**
>
> When incorporating the manufacturer's model into your LTSPICE simulation, you must adjust the value of the parallel capacitance C_P used in your Class-E design to account for the device capacitance.

Note that Figure 2.3 shows significant variation in C_{oss} near your operating voltage. Therefore, extracting an accurate value directly from the graph may be challenging. Use simulation-based tuning to refine your design.

2.3 Improved LTspice simulation

Update your simulation as follows:

- ☐ Repeat the LTSPICE simulation including
  - The manufacturer's MOSFET model
  - The complete equivalent inductor models extracted from your impedance measurements (Section 2.1).

The manufacturer's model captures the nonlinear capacitance behavior with reasonable accuracy. You may need to retune component values to achieve zero-voltage switching (ZVS), nominal output power, and maximum efficiency (N. Sokal and Amplifiers 2001). - [ ] Plot three full steady-state cycles of $v_g(t)$, $v_{ds}(t)$, and $v_{load}(t)$. - [ ] Report: - Simulated output power (updated simulation) - $\frac{\max(v_{ds}(t))}{V_i}$ - Drain efficiency - Maximum voltage across C_s - Power delivered to the MOSFET gate - Overall power amplifier efficiency - [ ] Update your component value table to reflect any tuning adjustments.

2.4 Power Amplifier stage build-up

As in previous labs, the PCB was designed using KiCad. The GitLab repository containing the design files and annotated schematic is available here.

> **Note**
>
> The boards include no external protection circuitry beyond what is internally provided in the ICs. This is intentional for simplicity. You are expected to fully understand the circuit operation and be able to diagnose and repair faults if necessary.

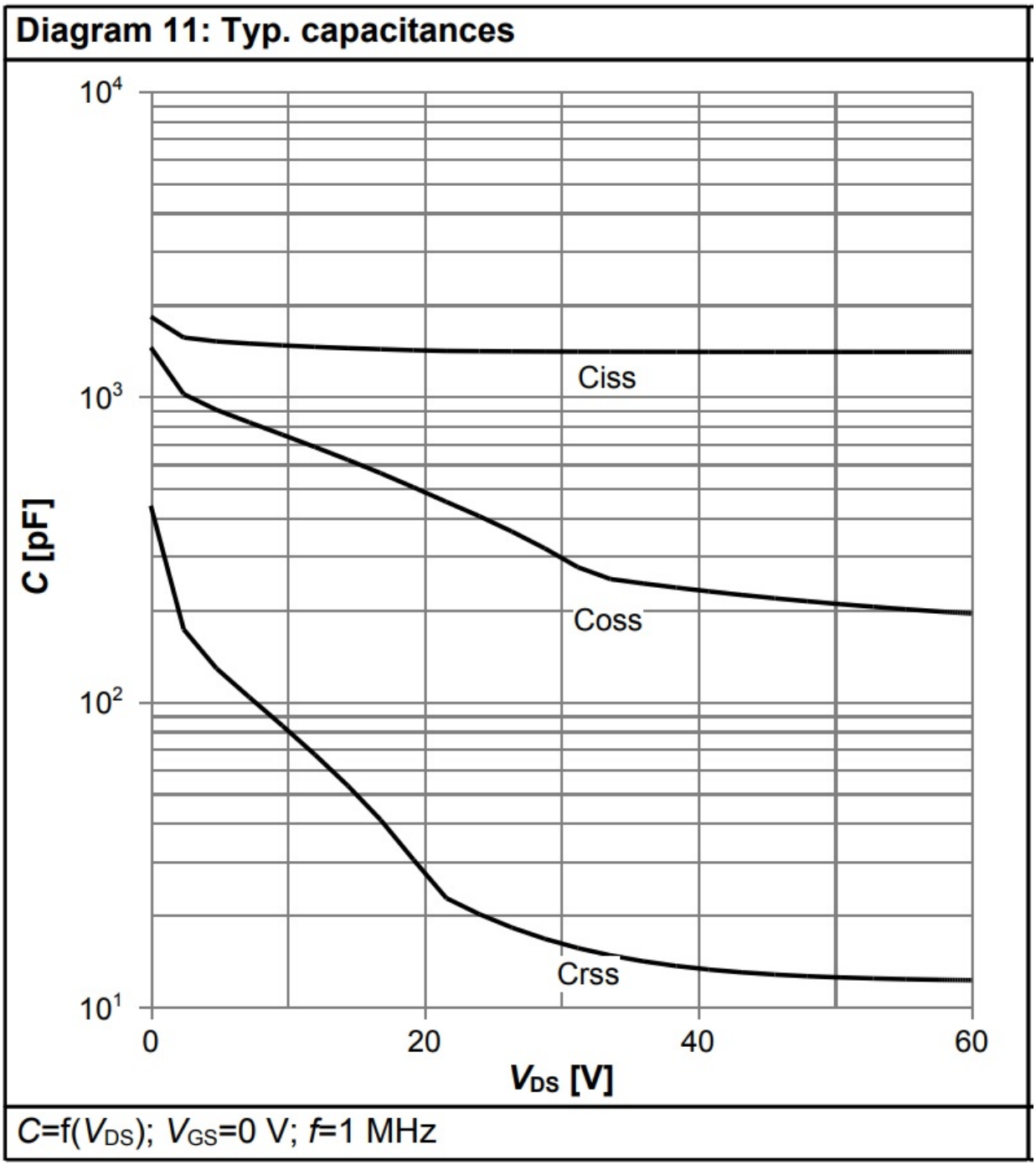


Figure 2.3: Device capacitance variation vs. drain voltage

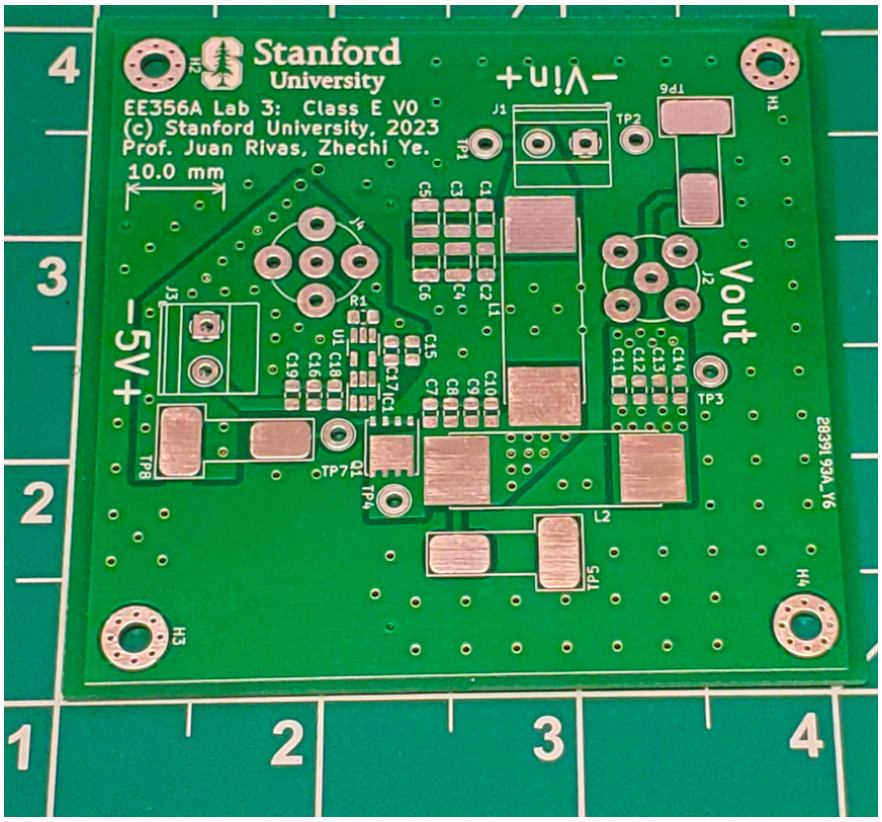


Figure 2.4: Empty PCB board

2.4.1 Assembly Procedure

- ☐ Starting with the empty PCB (Figure 2.4), place the inductors and capacitors for:
  - The Class-E network
  - The matching network
  - The input decoupling network that will ensure the input voltage remains steady and with low ripple
  - **Do not solder the MOSFET yet.**
- ☐ Using the NanoVNA, measure the impedance seen at the drain–source pads (MOSFET location) over $0.1\ \text{MHz} \leq f \leq 100\ \text{MHz}$.
- ☐ On a dB–log plot, compare:
  - The measured impedance
  - The simulated impedance (using an LTspice .AC analysis of the passive network only)

Use this comparison to identify discrepancies and adjust component values if necessary. After updating the simulation to reflect the actual board values, include the switch and gate driver models and verify ZVS operation in transient simulation.

2.5 Gate Drive Testing

In this lab, you will use the LM5114 gate driver from Texas Instruments. You can download the datasheet of the gate drive here.

A laboratory waveform generator will provide the input signal via SMA connector (J4).

2.5.1 Pre-Power Checks

After soldering:

- Inspect for solder bridges and loose solder balls.
- Clean the board with isopropyl alcohol (IPA).
- Wear gloves when performing surface-mount soldering.

2.5.2 Initial Gate Drive Test

Once the gate-board is assembled, test the gate drive by doing the following:

- ☐ **Verify correct orientation of polarized capacitors.**
- ☐ Use a DMM (continuity mode) to check for shorts.
- ☐ Connect the gate driver supply to 5 V.
- ☐ Set the function generator to:
  - $f = 6.78$ MHz
  - 0 V to 5 V square wave
  - 50% duty cycle
- ☐ Measure the gate driver output. You should observe a 6.78 MHz square wave with approximately 5 V peak amplitude.

> ⚠ Warning
>
> **Ensure the function generator output impedance is set to High Impedance. Failure to do so may damage the gate driver IC.**

After confirming proper operation:

- [ ]Install the Si MOSFET.
- ☐ Recheck for shorts.

☐ Fabricate three RF probe sockets for high-frequency measurements (TP5, TP6, TP8) to minimize probe ground inductance.

We need to be careful when doing these measurements by avoiding inserting a significant parasitic inductance. Sometimes, the ground lead of the oscilloscope probe inserts a lot of inductance that affects the measurement. We can improve your high frequency measurements by minimizing the length of the ground lead of the probe. This can be achieved by using a socket for your probe. This video shows a simple way to make a good oscilloscope probe socket.

2.6 Power Board Initial Check

Figure 2.5 shows the simplified experimental setup. The load will be an RF attenuator.

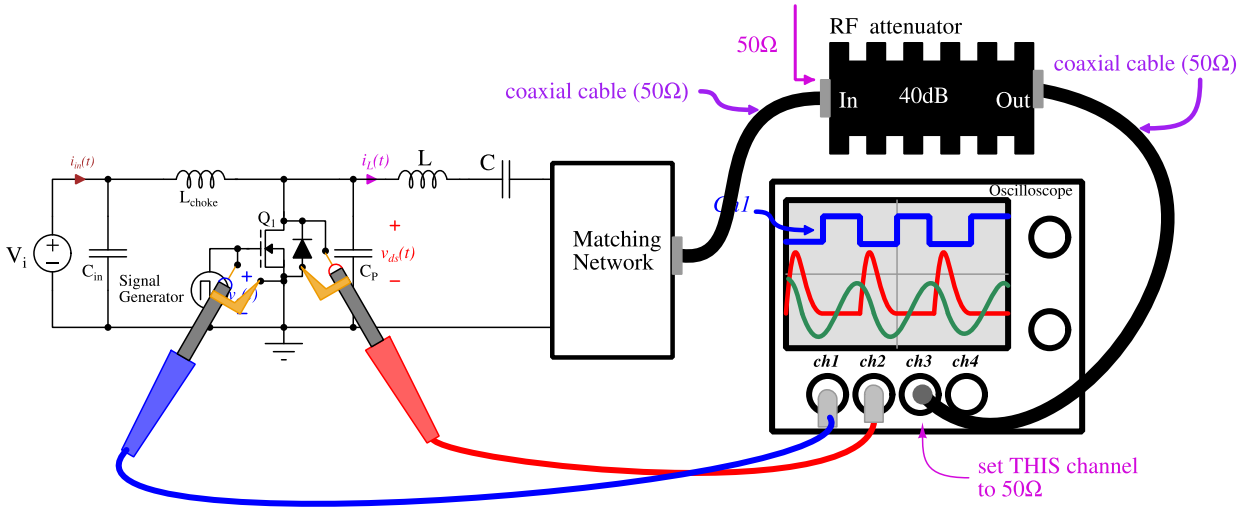


Figure 2.5: Experimental Setup (Simplified Schematic)

A 40 dB attenuator (Figure 2.6) terminated in $50\ \Omega$ presents a $50\ \Omega$ input impedance. Configure one oscilloscope channel to $50\ \Omega$ input impedance and use a $50\ \Omega$ coaxial cable. The measured signal will be attenuated by 40 dB.

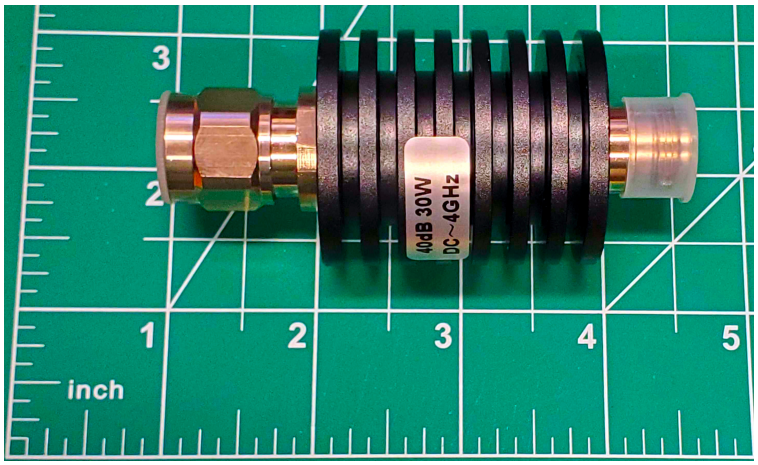


Figure 2.6: RF attenuator

2.6.1 Initial Power-Up Procedure

Once the board is completely assembled, do the following.

- ☐ **Verify correct polarity of all polarized capacitors.**
- ☐ Connect probes and attenuator to measure $v_g(t)$, $v_{ds}(t)$, and attenuated $v_{load}(t)$.
- ☐ Apply the 5 V gate-drive supply.
- ☐ Set the DC input to 0 V.
- ☐ Slowly increase the DC input from 0 V to 12 V.

Gradually increasing the input voltage reduces the risk of excessive dissipation during tuning. Additional tuning may be required to achieve ZVS and match simulated waveforms. **At lower input voltages, the nonlinear C_{oss} may be large enough to prevent ZVS. As the input voltage increases, the drain–source waveform should approach proper ZVS operation.**

> **!** Important
>
> After completing the lab, remember to return the oscilloscope channel input impedance to 1 MΩ.

Problem 3

Experimental Characterization of the power amplifier

3.1 Converter at Constant frequency

- ☐ Set the signal generator at 6.78 MHz and with a duty cycle of 50%. You will vary input V_i in the 5 V $\leq V_i \leq 13$ V every 2 V. Measure the input power and capture waveforms for the drain voltage and output voltage (don't forget to consider the attenuation factor of the attenuator).
- ☐ Plot P_o vs. V_i.
- ☐ Plot η vs. V_i.
- ☐ Plot the maximum $v_{ds}(t)$ vs. V_i
- ☐ Show captured waveforms of $v_g(t), v_{ds}(t)$ and $v_{load}(t)$ when $V_i = 5$ V, 9 V, and 13 V.
- ☐ Comment and compare the measurements to your simulation.

3.2 Converter operating at constant input voltage

- ☐ Set the $V_i = 12$ V and vary the frequency of the input to your gatedrive in the the 6.25 MHz $\leq fs \leq 7.25$ MHz every 100 kHz. Measure the input power and capture waveforms for the drain voltage and output voltage (don't forget to consider the attenuation factor of the attenuator).
- ☐ Plot P_o vs. V_i.
- ☐ Plot η vs. V_i.
- ☐ Show captured waveforms of $v_g(t), v_{ds}(t)$ and $v_{load}(t)$ when $f_s = 6.25$ MHz, 6.78 MHz, and 7.25 MHz.
- ☐ Comment and compare the measurements to your simulation.

> **!** Important
>
> Once you are done with the lab, please remember to change the channel impedance of the oscilloscope back to 1 MΩ!.

Problem 4

Checklist

Please show the following items to your CA and also upload them on Canvas. Put all the items in a single PDF file with your name and the lab session title at the top.

(Total points: 100).

- ☐ *(20 points)* Converter Design and simulation (Chapter 1)
- ☐ *(20 points)* Inductor design and characterization (Section 2.1)
- ☐ *(10 points)* Board construction and functional check: Check for good solder joints, a clean board and a clear and neat experimental setup.
- ☐ *(25 points)* Measurements and plots under constant frequency and varying input voltage (Section 3.1)
- ☐ *(25 point)* Measurements and plots under constant input voltage but varying switching frequency (Section 3.2)

Feedback

Please provide feedback to help improve future labs.

Acknowledgment

Thank you to Prof. Lei Gu, Zhechi Ye and Katherine Liang for their help putting together and testing the lab.

References

Sokal, N. O., and A. D. Sokal. 1975. “Class E-A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers.” *IEEE Journal of Solid-State Circuits* 10 (3): 168–76. https://doi.org/10.1109/JSSC.1975.1050582.

Sokal, NO, and Class-E RF Power Amplifiers. 2001. “QEX Commun.” Quart.